Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A receiver for use in a variable spreading factor-orthogonal frequency and code division multiplexing (VSF-OFCDM) system, said receiver being arranged to process a received signal having an associated chip rate, said receiver comprising:

a sequence extension remover for removing a predetermined number of chips from at least one predetermined position of said received signal to form a modified signal;

a first converter for converting the modified signal from a serial sequence to a parallel sequence;

a despreader coupled to said first converter for receiving said parallel sequence and for despreading said parallel sequence to derive a group of symbols;

an orthogonal transform block, coupled to said despreader for transforming said symbols from a first domain to form a transformed signal in a second domain;

an equalizer block coupled to said transform block for equalizing said transformed signal to reduce channel distortion and form an equalized signal;

a deinterleaver block coupled to said equalizer block to receive said equalized signal and form a deinterleaved signal; and

a second converter coupled to said deinterleaver block for converting said deinterleaved signal from a parallel sequence to a serial sequence.

2. (Original) The receiver according to claim 1, wherein said sequence extension remover is arranged to remove a predetermined number of chips carrying data denoting a cyclic prefix.

3. (Previously Presented) The receiver of claim 1, wherein said orthogonal transform block comprises a Fast Fourier Transform block.

4. (Previously Presented) The receiver of claim 1, wherein said first domain is the time domain and said second domain is the frequency domain.

5. (Previously Presented) The receiver of claim 1, wherein said despreader despreads said sequence to a symbol rate, said symbol rate being less than said chip rate at which said received signal was spread prior to being received by said receiver, the ratio of the chip rate to the symbol rate being the processing gain of the receiver.

6. (Previously Presented) A variable spreading factor-orthogonal frequency and code division multiplexing (VSF-OFCDM) system comprising one or more receivers according to claim 1.

7. (Original) A method of processing a received signal having an associated chip rate in a variable spreading factor-orthogonal frequency and code division multiplexing (VSF-OFCDM) system comprising the steps of:

removing a predetermined number of chips from at least one predetermined position of said received signal to form a modified signal;

converting the modified signal from a serial sequence to a parallel sequence;

despreading said parallel sequence to derive a group of symbols;

transforming in an orthogonal transform block said symbols from a first domain to form a transformed signal in a second domain;

equalizing said transformed signal to reduce channel distortion and form an equalized signal;

deinterleaving said equalized signal to form a deinterleaved signal; and

converting said deinterleaved signal from a parallel sequence to a serial sequence.

8. (Original) The method according to claim 7, wherein the step of removing said predetermined number of chips comprises removing chips carrying data denoting a cyclic prefix.

9. (Previously Presented) The method of claim 7, wherein the step of transforming said signal comprises applying a Fast Fourier Transform to said symbols.

10. (Previously Presented) The method of claim 7, wherein the step of transforming said symbols comprises transforming said symbols from the time domain to the frequency domain.

11. (Previously Presented) The method of claim 7, wherein the step of deinterleaving comprises forming a deinterleaved signal.

12. (Previously Presented) The method of claim 7, wherein the step of despreading comprises despreading said sequence to a symbol rate, said symbol rate being less than said chip rate at which said received signal was spread prior to being received by said receiver, the ratio of the chip rate to the symbol rate being the processing gain of the receiver.